C.) Amendments to the Specification:

Change Page 2, paragraph 5 to insert the patent numbers, by amending Page 2, paragraph 5 to read as follows:

[0005] The second known approach is using various source-synchronous techniques to align signal bits and the clock (such as "Dynamic Wave-pipelined Interface Apparatus and Methods Therefor." filed October 1999, IBM Patent 6654897 issued 25 Nov. 2003), as well as signal buffering and rotations at the receiver side (such as "An Elastic Interface Apparatus and Method Therefor." filed October 1999, IBM Patent 6334163 issued 25 Dec. 2001). Some of those source-synchronous interface and buffering techniques are very sophisticated, but these techniques are also complicated and their implementations require larger circuitry than the method and system of this invention.

Change "thorough" to "through" in line 17, page 5 by amending the paragraph 19 on page 5 to read as follows:

[0019] In case all *wc_ok*'s are at logic 1's, the NAND gate 316 output 318 of the Clock & Signal Select Control Logic 310 in FIG. 3 is at logic 0. The incoming bus signals Bit[0:N] instead of the output of FF1's 320-I through 320-N are selected as the input of FF2's 314-I through 314-N. The same clock used for Worst Delay Detect Logic 306-I through 306-N is selected as the clock for FF2's to capture the bus signals Bit[0:N].